Thermal Management

While the PCBs and components are being ordered, tested and shipped, time becomes available to focus on other parts of the project. In a presentation by the Phutung Research Institute concerning the broader perspective of detecting fecal contamination by means of Tryptophan-Like Fluorescence (TLF), light was shed on the challenge of thermal management in powering the LED actuator. There are two ways presented to configure the transducers to measure the TLF. Fig. 1 shows a 90 degree configuration where two PCBs are laid out orthogonally, however Fig. 2 shows an adjacent configuration where the PCBs are laid out in a planar fashion. The specific concern that is conveyed here is the influence of heat produced by the actuator to the sensitive receiver.

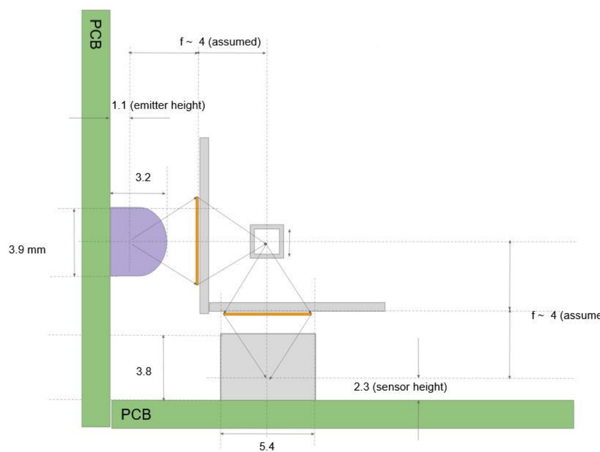

Fig 1. The 90° configuration using a square capillary tube

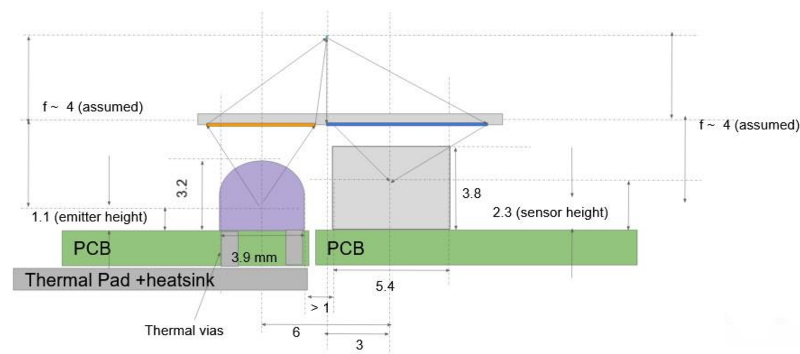

Fig 2. The adjacent configuration

Impact of heat on the components

An important part of an LED systems design is the system's ability to draw heat away from the LED junction. There are multiple reasons for this. High operating temperatures significantly reduce the performance of LEDs, namely in terms of a decreased light output and lifetime. [1] So regardless of the positioning of the LED, power dissipation in the form of heat would need to be drawn away from the junction for optimized performance. Besides the degrading performance on the emitter itself, the heat generated will also adversely affect the sensor depending on the type of sensor used.

Dark current

The photodiode used is a silicon photodiode. In terms of a temperature increase this typically translates to a doubling of the dark current for each 10K (or 10°C) increase. The shunt resistance approximately doubles for every 6K (or 6°C) increase. [2] The dark current at the increased temperature of Si Photodiodes can be modeled with formula (1).

$$I_{dk\,(T2)} = I_{dk\,(T1)} * 2^{\frac{(T2-T1)}{10}} \tag{1}$$

The source used [2] gives no clues as to which variable means what, but a quick verification provides all the information needed. Where $I_{dk\,(T1)}$ is the dark current of the specified temperature given on the datasheet, usually at 25°C. T2 is the expected temperature the photodiode will be operational at and T1 is the temperature provided on the datasheet. Since noise currents are generated as result of dark current, the higher the temperature, the higher the noise in the detector.

Spectral Response

An increase in temperature of a semiconductor shifts its absorption spectrum closer to longer wavelengths by reducing the band gap. The temperature-induced shifts only affect the responsivity significantly at the edges of the spectral responsivity curve, as shown in figure 3 from [2].

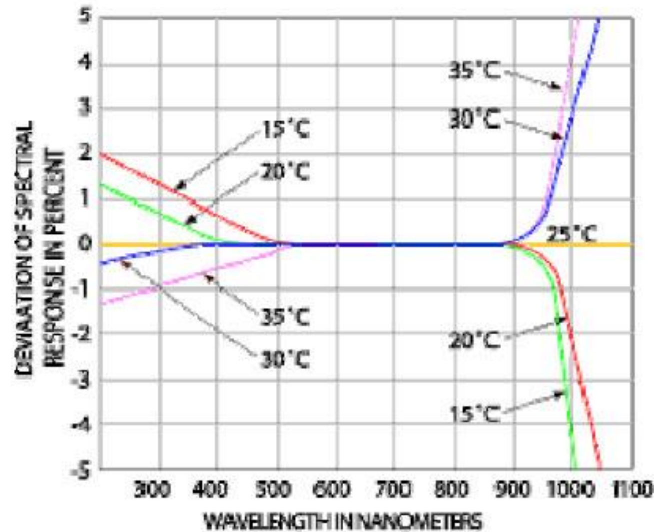

Fig. 3 Deviation of spectral response at different temperature changes in silicon

This behaviour can be explained by the absorption coefficient increase with the temperature. When the temperature increases, the absorption depth of light decreases. Consequently, the responsivity for short wavelengths has a negative temperature coefficient, since a significant amount of carriers could recombine and get lost in the heavily doped p-layer. As for longer wavelengths, responsivity has a positive

temperature coefficient, since more carriers will be generated in or near the depletion region of the pn-junction, and therefore increase the photocurrent. [3] So it seems the

Since the fluorescence that will be measured will be at 340-360nm, there will be a significant reduction in responsivity if the photodiode heats up beyond a certain point.

Determining maximum LED temperature

Looking at the datasheet of the IN-C39ATKU1, the UVC LED that will be used, a maximum junction temperature can be found in an absolute maximum ratings chart. [4] Chart as shown below.

Characteristics	Symbol	Min.	Typical	Max.	Unit
DC Forward Current[1]	IF	---	---	150	mA
Pulse Current (@1/10 duty) [2]	IP	---	---	TBD	mA
Forward Voltage	VF	5.0	---	9.0	V
Junction Temperature[3]	Tj	---	---	65	℃
Storage Temperature Range	Tstg	-40	---	80	℃
Soldering Temperature	Tsol	---	---	245	℃
Thermal Resistance Junction / Solder Point	Rth	---	15	---	℃/W
Viewing Angle[4]	2θ1/2	---	30/60/120	---	Deg

Notes:
1. When operating at other than ambient temperature, maximum allowable current depends on derating curves.
2. Pulse width = 0.01s & duty factor = 1/10.
3. When operating at maximum allowable current, Tj must be below 85 ℃.
4. Viewing angle tolerance is ± 10°.

Found is that the maximum junction temperature to be allowed is 65°C when operating at the maximum allowable current, which may not exceed 85°C.

The maximum allowable current is determined with the maximum forward current determination chart, as this changes with ambient temperature.

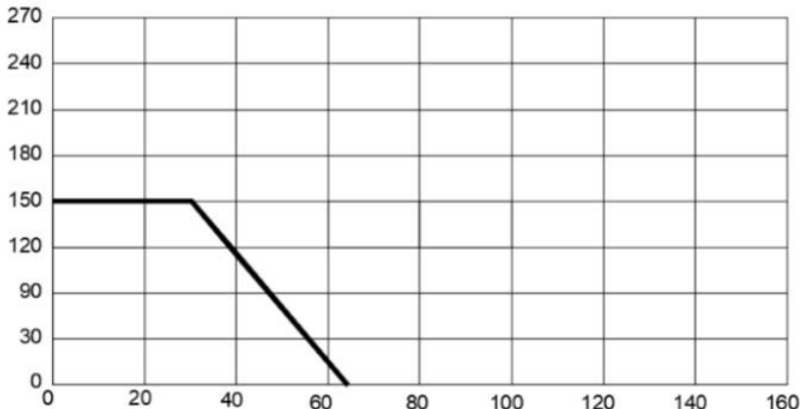

Fig 4. Plot of Allowable Forward Current vs. Ambient Temperature

Conclusion of heat limits

What can be concluded is that the maximum thermal requirements of the LED itself might be significantly less demanding than that of the photodiode. Since the 90° configuration has the transducers set further away from each other, this gives a clear advantage, in terms of thermal management, to this specific configuration. The only limiting factor would be the LED. Whereas with the planar configuration, the limiting factor would also be decided by the photodiode.

Heat transfer

The 90° configuration has the actuator and sensor placed far away enough as to not affect each other too much, but this does become a greater concern with the adjacent configuration. They are about 1mm apart from each other. The heat transfer from the LED to the photodiode would need to be calculated, as the limit of the heat would be set by the photodiode.

The net heat transfer rate [W] from one surface to another is approximated by (2)

$$\dot{Q}_{12} = \frac{\sigma({T_1}^4 - {T_2}^4)}{\frac{1-\varepsilon_1}{\varepsilon_1 A_1} + \frac{1}{A_1 F_{12}} + \frac{1-\varepsilon_2}{\varepsilon_2 A_2}} \tag{2}$$

Where ε_1 and ε_2 are the intensity of emitted radiation of surface one and two respectively, A_1 and A_2 the surface area of objects one and two respectively [m^2], F_{12} the view factor from surface one to two, δ the Stefan-Boltzmann constant [$W/(m^2K^4)$] and T_1 and T_2 the temperatures at object one and two respectively [K].

The Stefan-Boltzmann constant relates surface temperature to thermal radiation, with a constant value that equals $5.67\ 10^{-8}$ [$W/(m^2K^4)$].

View factor

“The view factor describes what fraction of a surface’s field-of-view is occupied by the opposing surface.” [5] This view factor from surface one to surface two (F_{12}) can be different than vice-versa (F_{21}). [5] Gives a reference to an online catalog of a substantial amount of view factors. One can be found of two parallel opposed cylinders of unequal radius and equal finite length. This is the closest approximation to the situation at hand that can be found. The catalog only displays a figure, some calculations and a chart, without any other context of the like. The catalog does show a reference to [6], which is the actual paper which describes a way how a ‘simple’ double-integral expression for the diffuse radiation view factor, F_{12}, between two parallel cylinders of finite lengths is derived. As shown in the figure below from the same paper. The paper goes into unrealistic territory where the cylinders are of infinite length, or where the radius of one of the cylinders approaches 0. Note that there is an assumption that both cylinders are of the same height, which in reality they are not.

The average of both are taken as the length of the cylinders. The same goes that the LED is modeled as a cylinder in this case, and not as half a globe atop a cylinder.

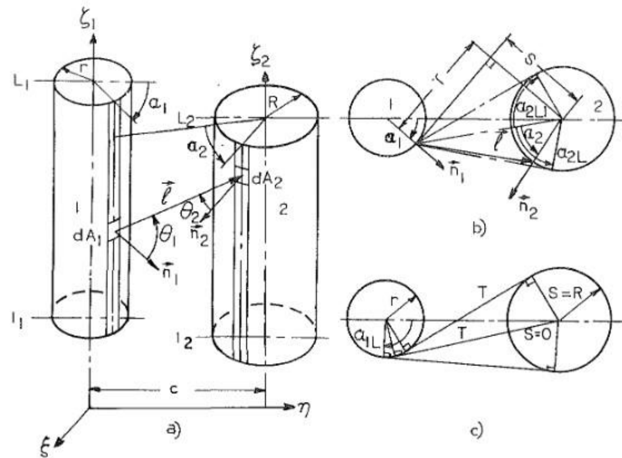

Fig. 1 Geometry for view factor analysis: (a) isometric view, (b) and (c) top view to define lengths, angles, limits of integration

Table 1 gives the details of the regions for which the approximations for finite cylinders may be applied with an accuracy of 1 percent or better. Here the planar configuration gives for r/R = 1.95/2.7 = 0.72, for L/R = (3.2+3.8)/2.7 = 1.3 and for S/R = 1/2.7 = 0.37. From this r/R is taken as 1, L/R as 1, and S/R as 0.5. Table 1, as seen below, provides that for F_{12}, equations 7 and 4 need to be multiplied for the desired outcome.

Table 1 The tabulated view factors are obtained by numerical integration. The view factors in the blank regions may be calculated by the equations shown with an error less than 1 percent.

r/R	L/R	$S/R = 0$	0.5	1.0	2.0
0	0.5	0.500	0.1037	0.0446	
	1.0		0.1526	0.0772	
	5.0				
	10.0		F_{12} = equations (8) × (5)		
	50.0				
.1	0.5	0.3453	0.0933	0.0415	
	1.0		0.1387	0.0721	
	5.0				
	10.0		F_{12} = equations (7) × (4)		
	50.0				
1.0	0.5	0.1440	0.0517	0.0264	
	1.0				
	5.0		F_{12} = equations (7) × (4)		
	10.0	0.1813			
	50.0	0.1834			
10.0	0.5	0.0233	0.0104	0.0062	0.0032
	1.0	0.0276	0.0167	0.0111	0.0062
	5.0	0.0344	0.0288	0.0246	0.0186
	10.0		F_{12} = equation (7) with		0.0229
	50.0		r and R interchanged × equation (4)		

Equation 4, as seen below, presents an analytical expression for the exact view factor derived by the crossed string method.

$$F_{12}^{\infty} = 0.5/\pi(\sqrt{(c/r)^2 - (R/r+1)^2} - \sqrt{(c/r)^2 - (R/r-1)^2} + \pi + (R/r-1)\cos^{-1}((R-r)/c) - (R/r+1)\cos^{-1}((R+r)/c)) \quad (4)$$

Filling in for c = 6, r = 1.95 and R = 2.7, gives $F^{\infty}_{12} = 0.0976$

Then taking equation 7, as seen below, to calculate the last bit of the desired F_{12} gives $F^{N}_{12} = 0.9063$

$$F_{12}^{N} = 1 - \frac{1}{\pi}\left\{\cos^{-1}\frac{C}{B} - \frac{R^2}{2rL}\left[\sqrt{(C + 2(R_0/R)^2)^2 - (2R_0/Rr/R)^2}\cos^{-1}\left(\frac{rC}{R_0 B}\right) + C\sin^{-1}\left(\frac{r}{R_0}\right) - \frac{\pi}{2}B\right]\right\} \quad (7)$$

where $C = (L/R)^2 - (R_0/R)^2 + (r/R)^2$, $B = (L/R)^2 + (R_0/R)^2 - (r/R)^2$ and

$$R_0/R = \sqrt{\frac{2\sqrt{c/R)^2 - 1} - \pi}{2\sin^{-1}\left(\frac{R}{c}\right)} + 1}$$ when n is eliminated.

As per table 1, we find for the view factor F_{12}

F_{12} = Equations (7) x (4) = 0.9063 * 0.0976 = 0.0885

Emissivity

As for thermal emittances for the surfaces used, [7] provides a table where the emittance of the LED can be found to be about 0.94. The thermal emittance of the photodiode would seem to be similar as that of a commercial sheet of aluminium, which has an emittance of 0.09.

The datasheet for the IN-C39ATKU1 gives no specifications for power dissipation, or for efficiency to calculate the power dissipated at any given time. However, in the thermal design notes in the datasheet, advised is to take the input power (I_F*U_F) as the power that will be dissipated. The fact that this is presented this way, tells us something about the efficiency of this particular LED.

Heatsink calculations

Thermal resistance R_ϑ, defined as heat rise [°C] divided by power transferred [W], is used to carry out heatsink calculations. [8] It's the reciprocal of heat conductance, similar to electrical resistance and electrical conductance. For power transferred entirely by heat conduction, the thermal resistance is a constant, independent of temperature, that depends only on the mechanical properties of the joint. For a succession of thermal joints, the total thermal resistance is the sum of the thermal resistances of the individual joints. As an example, for a transistor mounted to a heatsink, the total thermal resistance from transistor junction to the outside (ambient) world is the sum of the thermal resistance from junction to case $R_{\vartheta JC}$, the thermal resistance from case to heatsink $R_{\vartheta CS}$, and the thermal resistance from heatsink to ambient $R_{\vartheta SA}$. [8] The temperature of the junction is therefore

$$T_J = T_A + P(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) \tag{3}$$

Where T_A is the ambient temperature, and P is the power being dissipated. Since the LED will be mounted directly on a PCB, the thermal resistance from case to heatsink $R_{\vartheta CS}$ can be omitted. However, this might be replaced by the heat-conducting pad at the other end of the PCB. Also note that the PCB itself has a thermal resistance from the case to the thermal pad $R_{\vartheta CP}$, which needs to be taken into account. After this comes the thermal resistance from PCB to heatsink $R_{\vartheta PS}$. This eventually becomes

$$T_J = T_A + P(R_{\theta JC} + R_{\theta CP} + R_{\theta PS} + R_{\theta SA}) \tag{4}$$

An illustration (6) has been made to visualize this, so that these calculations become more intuitive to the reader. Note that the proportions are not representative to the scale of the real set-up.

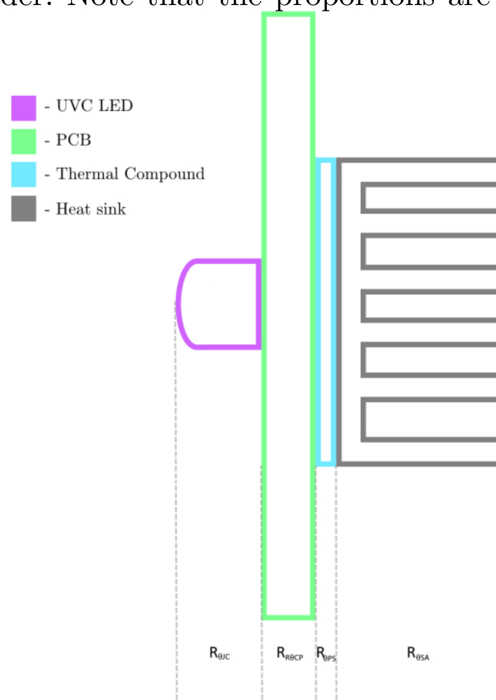

Fig 6. Visualization of the thermal resistance path

When looking at heatsinks, the maximum junction temperature T_J that is allowed is usually a given specification, where the total thermal resistance $R_{\vartheta JA}$ is needed. Transforming equation (4) gives

$$R_{\theta JA} = \frac{T_J - T_A}{P} \quad (5)$$

Equation (5) gives the maximum total thermal resistance from junction to ambient.

The multiple variables that are left open shows there is a great amount of flexibility to be had for the designer. Smaller heatsinks might be possible for instance, if the thermal resistance of the PCB is reduced. On the other side, a bigger heatsink or one with forced convection might be necessary in order to reduce the thermal conduction limitations of the PCB.

90° Configuration

An ambient temperature of around 23°C was laid down by PRI to be the norm in Nepal. However, since a higher ambient temperature puts more constrains on the thermal design, an ambient temperature of 25°C will be assumed, to be on the safe side. This assumption of the ambient temperature will only be beneficial, if the ambient temperature turns out to be lower.

The amount of watts dissipated by the LED depends on the efficiency. The IN-C39ATK states in the datasheet that "W = Input power (IF*VF)" and that "Tj = Ta + Rja*W". In the datasheet, the input power is used as the value where the dissipated heat would be used, so it is assumed in the datasheet that the efficiency is close to zero, so that the model of power dissipation takes the power at the input as the power being dissipated.
The maximum DC forward current at an ambient temperature of 25°C is 150mA, which correlates to a forward voltage of 7 volts. The input power then becomes 1.05W. Besides this, the datasheet provides the thermal resistance of the junction $R_{\vartheta JC}$, which is stated to be 15°C/W. Applying formula (4) with the assumption of an ambient temperature T_A of 25°C, with a power dissipation P of 1.05W and the junction thermal resistance $R_{\vartheta JC}$ of 15°C/W gives

$$T_J = 25 + 1.05(15 + R_{\theta CP} + R_{\theta PS} + R_{\theta SA})$$

Taking equation (5) into consideration, or shifting the variables from the function above, it can be found that the maximum allowable thermal resistance from junction to ambient must be no more than

$$R_{\theta JA} = \frac{65-25}{1.05} = 38°C/W.$$

Which, when filling in, gives

$$15 + R_{\theta CP} + R_{\theta PS} + R_{\theta SA} \leq 38°C/W$$

This leaves a combined maximum thermal resistance of 23°C/W for the remaining PCB, thermal compound, and heat sink.

Thermal Resistance of the PCB

The thermal resistance from the case to the thermal pad $R_{\vartheta CP}$ depends on the type of PCB being used. This has many variables, as this depends on things like PCB material, the amount of layers, the use of thermal vias and whether they are filled or not et cetera. [1]

To get a model of the thermal conductivity to certain types of PCBs, some calculations need to be done. The expression for thermal resistance through a solid volume is defined as [1][9]:

$$R_{\theta} = \frac{L}{k * A}$$

Where L is the layer thickness in [m], k is the thermal conductivity of the solid material in [W/m°C] or [W/mK], and A is the surface of the solid normal to the heat flow direction in [m^2]. Summing all layers up gives the thermal resistance of the total PCB.

A standard PCB has a thickness of about 1.6mm, but variations can be acquired. An area of 100m will be used as an example, combined with the 1.6mm thickness. Taking the thermal conductivity of each layer from [1] from the table below and calculating the R_{ϑ} for each layer gives

Table 3: Typical thermal conductivities of FR-4 board layers

Layer/Material	Thickness (µm)	Thermal conductivity (W/mK)
SnAgCu solder	75	58
Top layer copper	70	398
FR-4 dielectric	1588	0.2
Bottom layer copper	70	398
Electroless Nickel/Immersion Gold (ENIG)	5	4.2

$$\frac{75 \times 10^{-6}}{58 \times 0.0001} + \frac{70 \times 10^{-6}}{398 \times 0.0001} + \frac{1588 \times 10^{-6}}{0.2 \times 0.0001} + \frac{70 \times 10^{-6}}{398 \times 0.0001} + \frac{5 \times 10^{-6}}{4.2 \times 0.0001}$$

Which gives a thermal resistance of 79.4°C/W.

When taking an area of 300mm^2, with an area of 15x20mm for instance, the thermal resistance will be decreased down to 26,5°C/W. A significant change, so this will be looked at further.

When taking the area [m^2] as a variable in this equation to create formula (6), it can be seen in figure (5) that any change to the area over about 0,3m^2 will have a lot less effect than any change before that. Since heatsinking of an LED is considered, a PCB is assumed to be significantly smaller than 0,3m^2. This means any area increase would be highly beneficial to the lowering of the overall thermal resistance of the PCB.

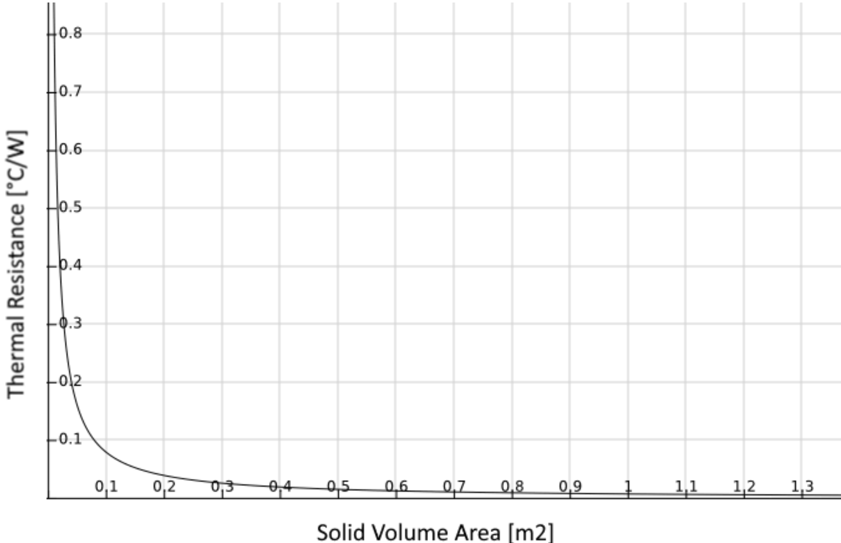

Fig 5. The plot of thermal resistance over solid volume area of the PCB

$$\frac{75\times10^{-6}}{58\,x}+\frac{70\times10^{-6}}{398\,x}+\frac{1588\times10^{-6}}{0.2\,x}+\frac{70\times10^{-6}}{398\,x}+\frac{5\times10^{-6}}{4.2\,x} \qquad (6)$$

However, both examples shown above already have a thermal resistance higher than the combined maximum thermal resistance as specified. So either the area needs to be sufficiently increased, allowing room for the thermal resistance of the heat sink and thermal compound, or there needs to be an implementation of techniques to lower the thermal resistance.

A way to lower thermal resistance could be done by using thermal vias, or using a different type of PCB altogether. This could be implemented with a metal core PCB (MCPCB) for instance, where the base metal material would help to spread the heat cropping up during operation.
Since cost-considerations are paramount, the option of implementing thermal vias will be looked at first, as MCPCBs are generally speaking more expensive. Thermal vias – Plated through-holes (PTH) between conductive layers is an inexpensive alternative in the goal to reduce thermal resistance. [1]

When N vias are used, which are solder-filled, the area increases by a factor of N_{vias}, which results in [1]

$$R_{\theta \text{vias}} = \frac{L}{N_{vias} * k * A}$$

However, this only applies to thermal vias directly normal to the heat source. The thermal resistance increases due to thermal spreading effects. [1] The thermal resistance of the FR-4 layer and the filled thermal vias are then treated to be in parallel with one another, as seen in the following equation

$$R_{\theta \text{vias // FR-4}} = \left(\frac{1}{R_{\theta \text{vias}}} + \frac{1}{R_{\theta \text{FR-4}}}\right)^{-1}$$

In deciding on the number of vias to use, real life tests have been done where the results showed that the number of vias beyond fourteen showed relatively insignificant improvements. [1] Besides this, the via radius will be taken as 0.2mm. The reason for this being that the area under the UVC LED needs to be able to accommodate the thermal vias. With an area of 1.35mm by 3.30mm, this leaves enough room for the vias to be placed in rows of two.

When filling in all equations, where use is made of table 5, a 300mm^2 board surface area, fourteen vias, and a via radius of 0.2mm, the closing equations come to be

$$R_{\theta \text{CP}} = \frac{75 \times 10^{-6}}{58\,x} + \frac{70 \times 10^{-6}}{398\,x} + \frac{1}{\frac{1}{\frac{1588 \times 10^{-6}}{14 \times 58\,\pi\,(0.2 \times 10^{-3})^2}} + \frac{1}{\frac{1588 \times 10^{-6}}{0.2\,x}}} + \frac{70 \times 10^{-6}}{398\,x}$$

$$\text{where } x = 0.0003$$

Which results in a total thermal resistance of 9.8°C/W.
If 0.3mm thermal vias are possible to implement, the total thermal resistance will decrease down to 5.5°C/W.

Table 5: Typical thermal conductivities of FR-4 board layers including thermal vias

Layer/Material	Thickness (µm)	Thermal conductivity (W/mK)
SnAgCu solder	75	58
Top-layer copper	70	398
FR-4	1588	0.2
Filled vias (SnAgCu)	1588	58
Bottom-layer copper	70	398
Solder mask (optional)	25	0.2

The result of 9.8°C/W will be taken as the final thermal resistance of the FR-4 PCB with fourteen thermal vias of 0.2mm. Filling this result in gives

$$15 + 9.8 + R_{\theta PS} + R_{\theta SA} \leq 38°C/W$$

which leaves a thermal resistance of

$$R_{\theta PS} + R_{\theta SA} \leq 13.2°C/W$$

For both the thermal compound and the heat sink.

Heat sink choice

In looking for an appropriate heat sink, some specifications are of importance. The dimensions should fit within the allocated space on the PCB, to fit appropriately. The thermal resistance is also of great importance, as this needs to be below the specified maximum.
A search for appropriate heat sinks at Digi-key leads to the BGAH190-090E heat sink as seen in figure (6).

Fig 6. The BGAH190-090E heat sink

The heat sink has a thermal resistance of about 7°C/W, and it's dimensions are 19 by 19 by 9.0mm. Something to note is that the thermal compound, thermal tape in this case, is included. So there is no need to worry about a third party thermal compound. Some alternative heat sinks could be the ATS-56001-C3-R0, or the ATS-52170G-C1-R0, if there are any issues with availability.

Conclusion

In conclusion, the calculations done indicate that the IN-C39ATK UVC LED can theoretically be kept within the specifications of a maximum of 65°C at the maximum specified supply current of 150mA, at an ambient temperature of 25°C, by implementing a low-cost two layer PCB with the use of fourteen filled-thermal vias with a diameter of 0.2mm and an appropriate heatsink.

Discussion

At some point the decision was made to focus more on the 90° configuration, because of the time-constraints. Note that the radiation calculations were already done, but natural convection influences needed to be looked at more closely. Since the planar configuration is not part of the first prototype, results were valued more and the decision was made to do the calculations necessary to keep the diode junction at a specified maximum temperature.

After consulting with different professors and existing literature, however, something came to light. It should be noteworthy that because of the heat in natural convection, the hot air rises and barely makes it to the photodiode next to it. That is, in theory, in practice this does happen because of the shifting of air currents, the humidity, the handling of the prototype, et cetera. [10] Therefore it is advised to not calculate the heat at the photodiode, but to measure it experimentally. Once this has been done, if necessary, further steps can be taken to reduce the heat at the photodiode.

The calculations have been done. Ideally, for the greatest chance of success, and to limit the amount of negative surprises, simulations should be done. This could for instance be done with a program like Autodesk Fusion 360.

Because of time-constraints, no calculations were done on the use of MCPCBs. This could be looked at, to more efficiently draw away heat from the junction of the LED, if necessary. This comes with a higher PCB price though, and doesn't seem necessary with the use of a two-layer PCB with thermal vias.

No further research was done on contact surfaces and thermal interference, in particular the use of different thermal compounds. This might be worth looking into, but as the designers choice heat sinks already come with their own, it seems rather redundant. When or if it becomes necessary to look further into thermal compounds, the basics are well laid out in [11].

The final thing to add is that the electronics used to drive the UVC LED also have a specified maximum temperature they can reliably work at. It is unlikely that the 65°C will go over this specified limit, but if it does, there are two ways of solving that issue. One way would be to have a separate PCB to power the LED, and create a direct connection to the LED PCB. The heat will not be distributed to the electronics driving the LED. This would be an easy solution to design, but might be more costly in manufacturing.
Another way to solve this would be to look into the thermal conductivity through multilayer PCBs. There is a paper going in-depth into the design of this [12], to reduce the heat spreading to critical components within the same PCB.

Sources

[1] *Optimizing PCB Thermal Performance for Cree® XLamp® LEDs*, Cree Inc., 2019.
[2] "Optical Detectors," National Tsing Hua University, Department of Power Mechanical Engineering, Wei-Chih Wang. [Online]. Available: https://depts.washington.edu/mictech/optics/me557/detector.pdf [Accessed: May. 5, 2021].
[3] "Temperature and Bias Effects," Frequently Asked Questions | OSI Optoelectronics. [Online]. Available: https://www.osioptoelectronics.com/technology-corner/frequently-asked-questions/temperature-bias-effects.aspx#01. [Accessed: Jun. 10, 2021].
[4] Inolux, "IN-C39ATK / IN-C39BTK / IN-C39CTK UVC Series", Aug. 10 2019. Silicon Valley, Available: http://www.inolux-corp.com/datasheet/Inolux%20UV/IN-C39(X)TK%20UVC%20Series%20V1.2.pdf [Accessed: May 4, 2021].
[5] "Radiation," Chapter 1, The Dutch Society for Precision Engineering. [Online]. Available: https://www.dspe.nl/knowledge-base/thermomechanics/chapter-1-basics/1-2-heat-transfer/radiation/ [Accessed: Jun 8, 2021].
[6] View Factors in Radiation Between Two Parallel Oriented Cylinders of Finite Lengths, N.H.Juul, Journal of Heat Transfer, P. 384-388, 1982.
[7] A Heat Transfer Textbook Fifth Edition, John H. Lienhard IV and John H. Lienhard V, 2020, table 10.1.
[8] The Art of Electronics 3rd Edition, Paul Horowitz and Winfield Hill, 2017.
[9] Modeling of Thermal Via Heat Transfer Performance for Power Electronics Cooling, Catalin Negrea and Paul Svasta, 2011 IEEE.
[10] Adrian Bejan, Heat Transfer, John Wiley & Sons, 1993.
[11] Thermal Interface Material Comparison: Thermal Pads vs. Thermal Grease, AMD, April 2004.
[12] Design of Anisotropic Thermal Conductivity in Multilayer Printed Circuit Boards, Ercan M. Dede, Paul Schmalenberg, Tsuyoshi Nomura and Masanori Ishigaki, December 2015 IEEE.